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Jameco Part Number 125495

Embedded Pentium® Processor

100 MHz, 133 MHz, 166 MHz

Datasheet

Product Features

- Compatible with Large Software Base
  - — MS-DOS*, Windows*, OS/2*, UNIX*
- 32-Bit Processor with 64-Bit Data Bus
- Superscalar Architecture
  - — Two Pipelined Integer Units are Capable of Two Instructions/Clock
  - — Pipelined Floating-Point Unit
- Separate Code and Data Caches
  - — 8-Kbyte Code, 8-Kbyte Write-Back Data
  - — MESI Cache Protocol
- Advanced Design Features
  - — Branch Prediction
  - — Virtual Mode Extensions
- 3.3 V BiCMOS Silicon Technology
- 4-Mbyte Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Dual Processing Configuration
- Functional Redundancy Checking Support
- Internal Error Detection Features
- Multiprocessor Support
  - — Multiprocessor Instructions
  - — Support for Second-level Cache
- On-Chip Local APIC Controller
  - — Multiprocessor Interrupt Management
  - — 8259 Compatible
- Power Management Features
  - — System Management Mode
  - — Clock Control
- Fractional Bus Operation
  - — 166-MHz Core/66-MHz Bus
  - — 133-MHz Core/66-MHz Bus
  - — 100-MHz Core/66-MHz Bus
- iCOMP® Index 2.0 Rating†
  - — 127 at 166 MHz
  - — 111 at 133 MHz
  - — 90 at 100 MHz

†Contact Intel Corporation for more information about iCOMP® Index 2.0 ratings.

The embedded Pentium® processor provides high performance for embedded applications. The Pentium processor is compatible with the entire installed base of applications for DOS*, Windows*, OS/2*, and UNIX*.

The Pentium processor superscalar architecture can execute two instructions per clock cycle. Branch prediction and separate code and data caches also increase performance. The pipelined floating-point unit delivers a high level of performance. Separate code and data caches reduce cache conflicts while remaining software transparent. The Pentium processor has 3.3 million transistors and is built on Intel's advanced 3.3 V BiCMOS silicon technology. The Pentium processor has on-chip dual processing support, a local multiprocessor interrupt controller, and SL power management features.

Order Number: 273202-001
November 1998

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Revision History

Date	Revision	Description
11/12/98	001	This is the first publication of this document.

1.0 Architecture Overview

The Intel® embedded Pentium® processor is binary compatible with the 8086/88, 80286, Intel386™ DX, Intel386 SX, Intel486™ DX, Intel486 SX, IntelDX2™, IntelDX4™ and 60/66 MHz Pentium processors.

The embedded Pentium processor family consists of the following products:

- Embedded Pentium processors (described in this document).
  - — Pentium processor at 166 MHz, iCOMP Index 2.0 rating = 127
  - — Pentium processor at 133 MHz, iCOMP Index 2.0 rating = 111
  - — Pentium processor at 100 MHz, iCOMP Index 2.0 rating = 90
- Pentium processor with Voltage Reduction Technology (described in a separate datasheet, order number 273203).
  - — Pentium processor with Voltage Reduction Technology at 133 MHz, iCOMP Index 2.0 rating = 111

Pentium processor features include:

- Superscalar architecture
- Dynamic branch prediction
- Pipelined floating-point unit
- Improved instruction execution time
- Separate 8-Kbyte code and 8-Kbyte data caches
- Writeback MESI protocol in the data cache
- 64-Bit data bus
- Bus cycle pipelining
- Address parity
- Internal parity checking
- Functional redundancy checking
- Execution tracing
- Performance monitoring
- IEEE 1149.1 boundary scan
- System Management Mode
- Virtual Mode extensions
- Fractional bus operation allowing higher core frequency operation
- Dual processing support
- SL power management features
- On-chip local APIC device

1.1 Pentium® Processor Family Architecture

The application instruction set of the Pentium processor family includes the complete Intel486 processor family instruction set with extensions to accommodate some of the additional functionality of the Pentium processor. All application software written for the Intel386 and Intel486 family microprocessors runs on Pentium processors without modification. The on-chip memory management unit is completely compatible with the Intel386 family and Intel486 family of processors.

Pentium processors implement several enhancements to increase performance. The two instruction pipelines and the floating-point unit are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating-point instruction (under certain circumstances, two floating-point instructions) in one clock.

Branch prediction is implemented in Pentium processors. To support this, the processor has two prefetch buffers: one prefetches code in a linear fashion and the other prefetches code according to the BTB so the needed code is almost always prefetched before it is needed for execution.

The floating-point unit (FPU) is up to ten times faster than the FPU used on the Intel486 processor for common operations including add, multiply, and load.

Pentium processors include separate code and data caches integrated on-chip to meet performance goals. Each cache is 8 Kbytes with a 32-byte line size, and is two-way set associative. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be write back or write through on a line-by-line basis and follows the MESI protocol. The data cache tags are triple-ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are also triple-ported to support snooping and split-line accesses. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The caches can be enabled or disabled by software or hardware.

Pentium processors have a 64-bit data bus for fast data transfer. Burst read and burst write back cycles are supported. In addition, bus cycle pipelining allows two bus cycles to occur simultaneously. The Memory Management Unit contains optional extensions to the architecture which allow 2-Mbyte and 4-Mbyte page sizes.

Pentium processors have added significant data integrity and error detection capability. Data parity checking is still supported on a byte-by-byte basis. Address parity checking and internal parity checking features have been added along with a new exception, the machine check exception.

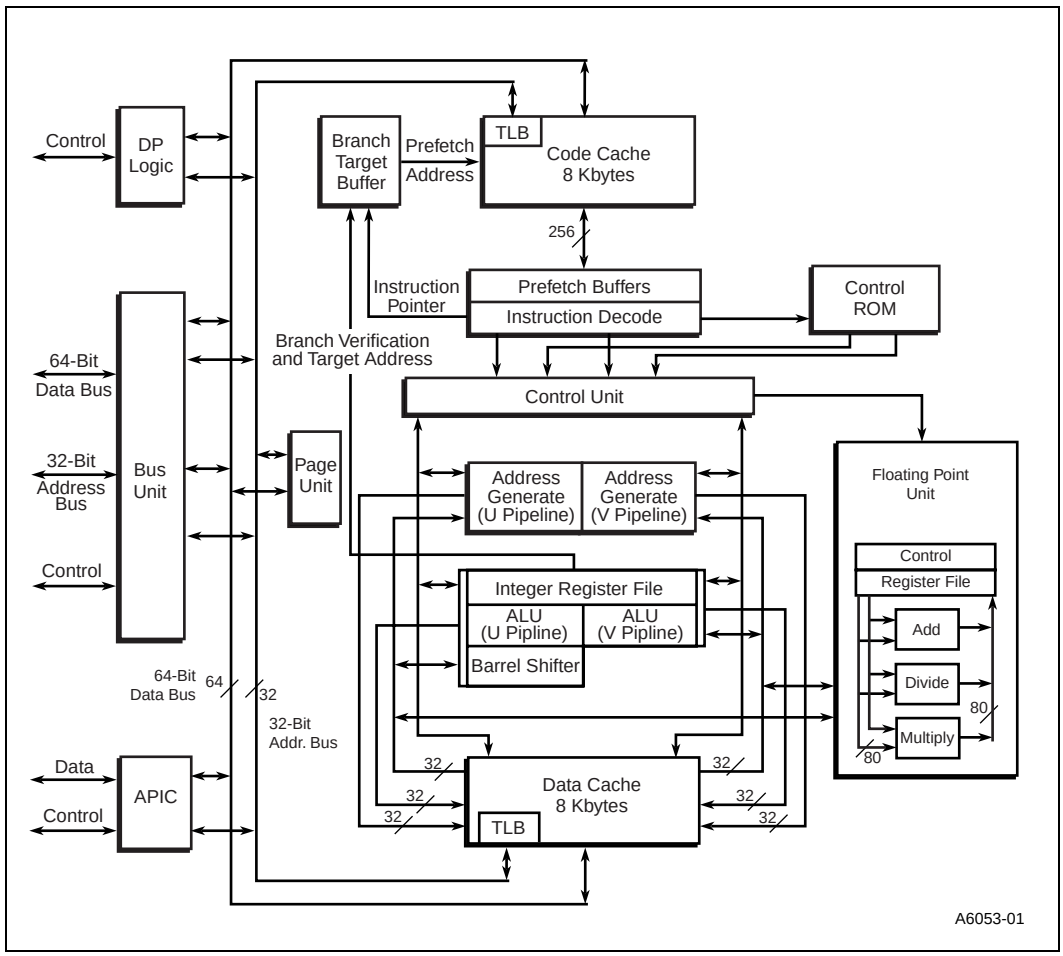
Pentium processors offer functional redundancy checking to provide maximum error detection of the processor and the interface to the processor. When functional redundancy checking is used, a second processor, the “checker” executes in lock-step with the “master” processor. The checker samples the master’s outputs, compares those values with the values it computes internally, and asserts an error signal when a mismatch occurs.

As more and more functions are integrated on-chip, the complexity of board level testing is increased. To address this, Pentium processors provide test and debug capability. Pentium processors implement IEEE Boundary Scan (Standard 1149.1). In addition, Pentium processors provide four breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. Execution tracing provides external indications when an instruction has completed execution in either of the two internal pipelines, or when a branch has been taken.

System Management Mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to the virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a virtual 8086 monitor.

Figure 1 is a block diagram of the embedded Pentium processor.

Figure 1. Embedded Pentium® Processor Block Diagram



The block diagram shows the two instruction pipelines, the “u” pipe and the “v” pipe. The u-pipe can execute all integer and floating-point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

The separate code and data caches are shown in the block diagram. The data cache has two ports, one for each of the two pipes (the tags are triple-ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so the processor can execute the instruction. The control ROM contains microcode to control the sequence of operations that must be performed to implement the Pentium processor architecture. The control ROM unit has direct control over both pipelines.

Pentium processors contain a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

Symmetric dual processing in a system is supported with two Pentium processors. The two processors appear to the system as a single processor. Operating systems with dual processing support properly schedule computing tasks between the two processors. This scheduling of tasks is transparent to software applications and the end-user. Logic built into the processors supports a "glueless" interface for easy system design. Through a private bus, the two Pentium processors arbitrate for the external bus and maintain cache coherency. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies.

In this document, in order to distinguish between two Pentium processors in dual processing mode, one processor is the "Primary" processor and the other is the "Dual" processor. Note that this is a different concept than that of "master" and "checker" processors described in the discussion on functional redundancy on page 8.

The Pentium processor supports clock control. When the clock to the processor is stopped, power dissipation is virtually eliminated. This makes the Pentium processor a good choice for energy-efficient designs.

The Pentium processor supports fractional bus operation. This allows the processor core to operate at high frequencies, while communicating with the external bus at lower frequencies.

The Pentium processor contains an on-chip Advanced Programmable Interrupt Controller (APIC). This APIC implementation supports multiprocessor interrupt management (with symmetric interrupt distribution across all processors), multiple I/O subsystem support, 8259A compatibility, and inter-processor interrupt support.

Pentium processor architectural features are described in more detail in the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204).

1.2 Pentium® Processors with Voltage Reduction Technology

The Embedded Pentium processor with Voltage Reduction Technology is described in the *Embedded Pentium® Processor with Voltage Reduction Technology* datasheet (order number 273203).

2.0 Packaging Information

2.1 Pentium® Processor Pinout

Figure 2. Pentium® Processor SPGA Package Pinout (Top Side View)

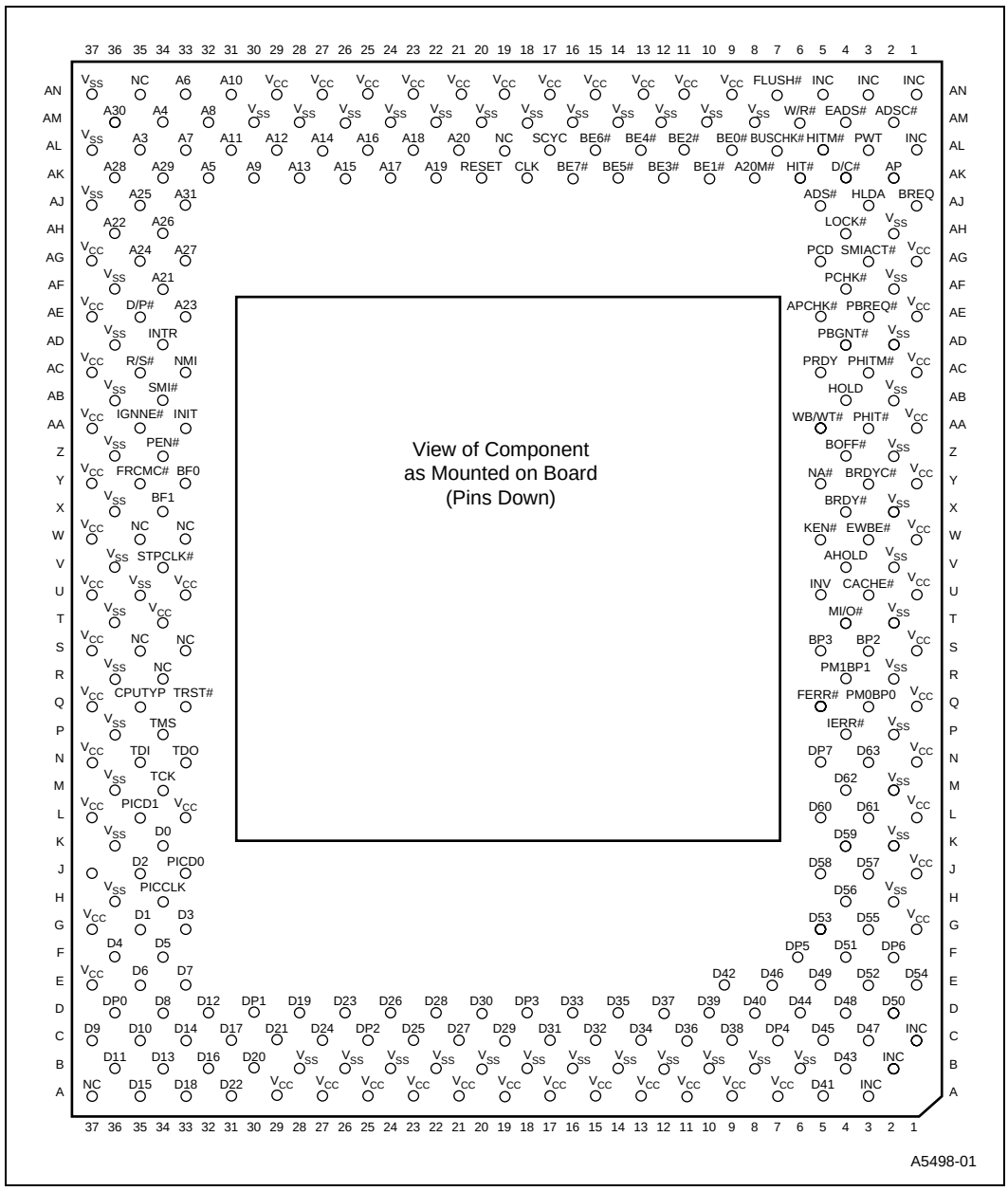
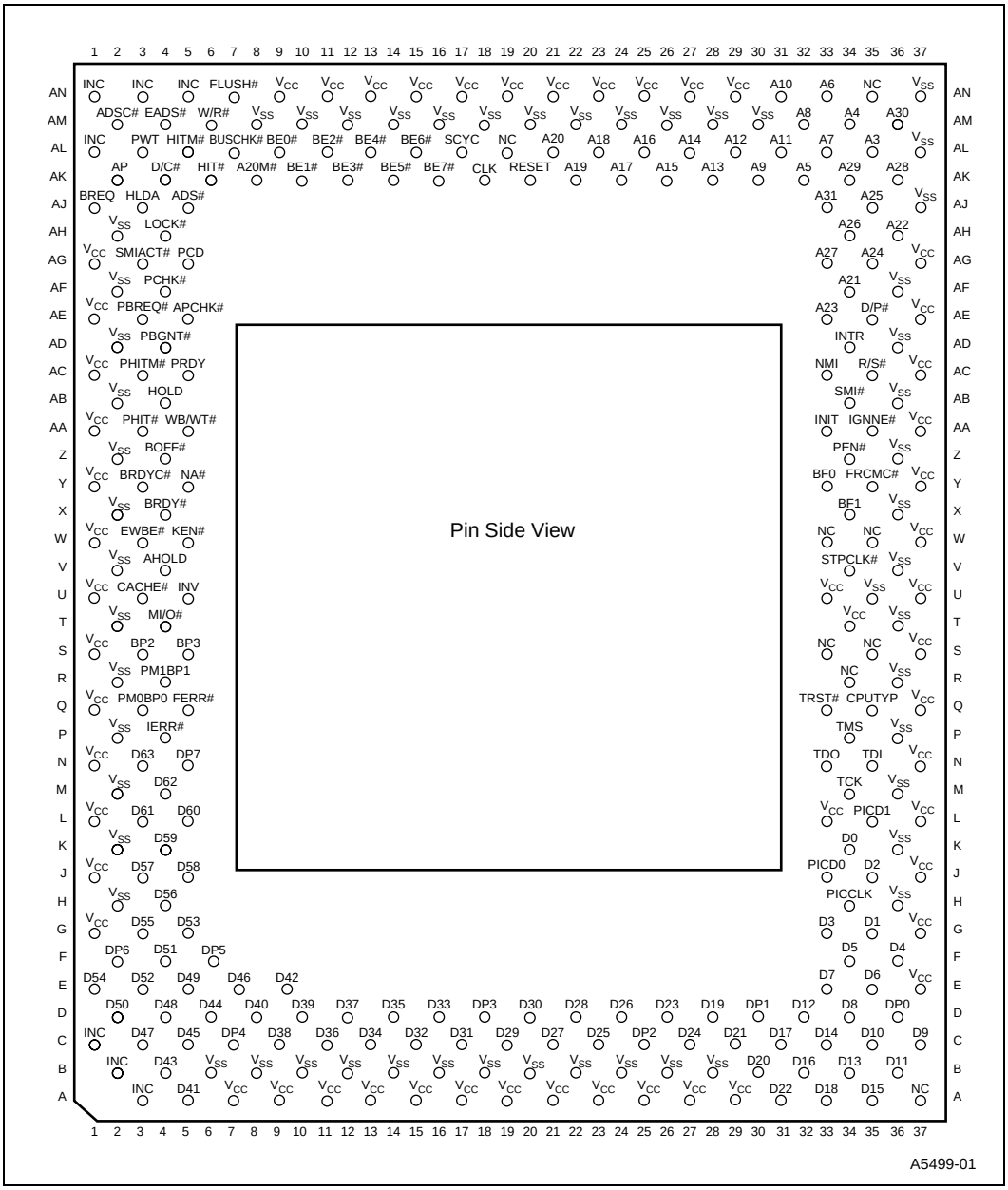


Figure 3. Pentium® Processor SPGA Package Pinout (Pin Side View)


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37
AN INC INC INC FLUSH# VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC A10 A6 NC VSS
AM ADSC# EADS# W/R# VSS VSS VSS VSS VSS VSS VSS VSS VSS VSS VSS VSS A8 A4 A30
AL INC PWT HITM# BUSCHK# BE0# BE2# BE4# BE6# SCYC NC A20 A18 A16 A14 A12 A11 A7 A3 VSS
AK AP D/C# HIT# A20M# BE1# BE3# BE5# BE7# CLK RESET A19 A17 A15 A13 A9 A5 A29 A28
AJ BREQ HLDA ADS# A31 A25 VSS
AH VSS LOCK# A26 A22
AG VCC SMIACT# PCD A27 A24 VCC
AF VSS PCHK# A21 VSS
AE VCC PBREQ# APCHK# A23 D/P# VCC
AD VSS PBGNT# INTR VSS
AC VCC PHITM# PRDY NMI R/S# VCC
AB VSS HOLD SMI# VSS
AA VCC PHIT# WB/WT# INIT IGNNE# VCC
Z VSS BOFF# PEN# VSS
Y VCC BRDYC# NA# BF0 FRCMC# VCC
X VSS BRDY# BF1 VSS
W VCC EWBE# KEN# Pin Side View NC NC VCC
V VSS AHOLD STPCLK# VSS
U VCC CACHE# INV VCC VSS VCC
T VSS MI/O# VCC VSS
S VCC BP2 BP3 NC NC VCC
R VSS PM1BP1 NC VSS
Q VCC PM0BP0 FERR# TRST# CPUTYP VCC
P VSS IERR# TMS VSS
N VCC D63 DP7 TDO TDI VCC
M VSS D62 TCK VSS
L VCC D61 D60 VCC PICD1 VCC
K VSS D59 D0 VSS
J VCC D57 D58 PICD0 D2 VCC
H VSS D56 PICCLK VSS
G VCC D55 D53 D3 D1 VCC
F DP6 D51 DP5 D5 D4
E D54 D52 D49 D46 D42 D7 D6 VCC
D D50 D48 D44 D40 D39 D37 D35 D33 DP3 D30 D28 D26 D23 D19 DP1 D12 D8 DP0
C INC D47 D45 DP4 D38 D36 D34 D32 D31 D29 D27 D25 DP2 D24 D21 D17 D14 D10 D9
B INC D43 VSS VSS VSS VSS VSS VSS VSS VSS VSS VSS VSS VSS VSS VSS VSS VSS D20 D16 D13 D11
A INC D41 VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC D22 D18 D15 NC
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37
A5499-01

2.1.1 Pin Cross Reference

Table 1. Pin Cross-Reference by Pin Name — Address and Data Pins

Pin	Location	Pin	Location	Pin	Location	Pin	Location	Pin	Location
Address									
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		
Data									
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Table 2. Pin Cross-Reference by Pin Name — Control Pins

Pin	Location	Pin	Location	Pin	Location	Pin	Location
A20M#	AK08	BRDYC#	Y03	FLUSH#	AN07	PEN#	Z34
ADS#	AJ05	BREQ	AJ01	FRCMC#	Y35	PM0/BP0	Q03
ADSC#	AM02	BUSCHK#	AL07	HIT#	AK06	PM1/BP1	R04
AHOLD	V04	CACHE#	U03	HITM#	AL05	PRDY	AC05
AP	AK02	CPUTYP	Q35	HLDA	AJ03	PWT	AL03
APCHK#	AE05	D/C#	AK04	HOLD	AB04	R/S#	AC35
BE0#	AL09	D/P#	AE35	IERR#	P04	RESET	AK20
BE1#	AK10	DP0	D36	IGNNE#	AA35	SCYC	AL17
BE2#	AL11	DP1	D30	INIT	AA33	SMI#	AB34
BE3#	AK12	DP2	C25	INTR/ LINT0	AD34	SMIACT#	AG03
BE4#	AL13	DP3	D18	INV	U05	TCK	M34
BE5#	AK14	DP4	C07	KEN#	W05	TDI	N35
BE6#	AL15	DP5	F06	LOCK#	AH04	TDO	N33
BE7#	AK16	DP6	F02	M/IO#	T04	TMS	P34
BOFF#	Z04	DP7	N05	NA#	Y05	TRST#	Q33
BP2	S03	EADS#	AM04	NMI/LINT1	AC33	W/R#	AM06
BP3	S05	EWBE#	W03	PCD	AG05	WB/WT#	AA05
BRDY#	X04	FERR#	Q05	PCHK#	AF04		
APIC							
PICCLK	H34	PICD0/ [DPEN#]	J33	PICD1/ [APICEN]	L35		
Clock Control							
CLK	AK18	BF0	Y33	BF1	X34	STPCLK#	V34
Dual Processor Private Interface							
PBGNT#	AD04	PBREQ#	AE03	PHIT#	AA03	PHITM#	AC03

Table 3. Pin Cross-Reference by Pin Name — Power, Ground and No Connect Pins

V_{CC}								
A07	A19	E37	L33	S01	W01	AC01	AN09	AN21
A09	A21	G01	L37	S37	W37	AC37	AN11	AN23
A11	A23	G37	N01	T34	Y01	AE01	AN13	AN25
A13	A25	J01	N37	U01	Y37	AE37	AN15	AN27
A15	A27	J37	Q01	U33	AA01	AG01	AN17	AN29
A17	A29	L01	Q37	U37	AA37	AG37	AN19	
V_{SS}								
B06	B18	H02	P02	U35	Z36	AF36	AM12	AM24
B08	B20	H36	P36	V02	AB02	AH02	AM14	AM26
B10	B22	K02	R02	V36	AB36	AJ37	AM16	AM28
B12	B24	K36	R36	X02	AD02	AL37	AM18	AM30
B14	B26	M02	T02	X36	AD36	AM08	AM20	AN37
B16	B28	M36	T36	Z02	AF02	AM10	AM22	
NC/INC†								
A03	B02	R34	S35	W35	AL19	AN03	AN35	
A37	C01	S33	W33	AL01	AN01	AN05		

† These pins should be left unconnected. Connection of these pins may result in component failure or incompatibility with processor steppings.

2.1.2 Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active high inputs should be connected to GND. No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

2.1.3 Pin Quick Reference

This section gives a brief functional description of each of the pins. For a detailed description, see the *Pentium® Processor Family Developer's Manual* (order number 273204).

Note: All input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level. Square brackets around a signal name indicate that the signal is defined only at RESET.

The following pins become I/O pins when two Pentium processors are operating in a dual processing environment:

- ADS#, CACHE#, HIT#, HITM#, HLDA#, LOCK#, M/IO#, D/C#, W/R#, SCYC

Table 4. Pin Quick Reference (Sheet 1 of 5)

Symbol	Type†	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the processor emulates the address wraparound at 1 Mbyte that occurs on the 8086 by masking physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode. A20M# is internally masked by the processor when configured as a Dual processor.
A31–A3	I/O	As outputs, the **address lines** of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31–A5.
ADS#	O	The **address strobe** indicates that a new valid bus cycle is currently being driven by the processor.
ADSC#	O	The **additional address strobe** signal is functionally identical to ADS#. This signal can be used to relieve tight board timings by easing the load on the ADS# signal.
AHOLD	I	In response to the assertion of **address hold**, the processor stops driving the address lines (A31–A3), and AP in the next clock. The rest of the bus remains active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the processor with even parity information on all processor generated cycles in the same clock in which the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that the correct parity check status is indicated by the processor.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the processor has detected a parity error on the address bus during inquire cycles. APCHK# remains active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	**Advanced programmable interrupt controller enable** enables or disables the on–chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the PICD1 signal.
BE7#–BE5# BE4#–BE0#	O I/O	The **byte enable** pins determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31–A3). The lower four byte enable pins (BE3#–BE0#) are used as APIC ID inputs and are sampled at RESET. In dual processing mode, BE4# is used as an input during Flush cycles.
BF1–BF0	I	**Bus frequency** determines the bus-to-core frequency ratio. BF1–BF0 are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF1–BF0 must not change values while RESET is active. See Table 5 for bus frequency selections.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor floats all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the processor restarts the aborted bus cycle(s) in their entirety.
BP3–BP2 PM1/BP1– PM0/BP0	O	The **breakpoint** pins (BP3–BP0) correspond to the debug registers, DR3–DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.

† The pins are classified as Input or Output based on their function in Master Mode. See the *Pentium® Processor Family Developer's Manual* (order number 273204) for more information.

Table 4. Pin Quick Reference (Sheet 2 of 5)

Symbol	Type†	Name and Function
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	The **additional burst ready** signal has the same functionality as BRDY#. This signal can be used to relieve tight board timings by easing the load on the Burst Ready signal.
BREQ	O	The **bus request** output indicates to the external system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. When this pin is sampled active, the processor latches the address and control signals in the machine check registers. When BUSCHK# is asserted and the MCE bit in CR4 is set, the processor vectors to the machine check exception. To ensure that BUSCHK# is always recognized, STPCLK# must be deasserted any time BUSCHK# is asserted by the system, before the system allows another external bus cycle. When BUSCHK# is asserted by the system for a snoop cycle while STPCLK# remains asserted, normally (when MCE=1) the processor vectors to the exception after STPCLK# is deasserted. When another snoop to the same line occurs during STPCLK# assertion, the processor can lose the BUSCHK# request.
CACHE#	O	For processor-initiated cycles, the **cacheability** pin indicates internal cacheability of the cycle (if a read), and indicates a burst write back cycle (if a write). When this pin is driven inactive during a read cycle, the processor does not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor's external bus, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD1–PICD0 are specified with respect to the rising edge of CLK. It is recommended that CLK begin toggling within 150 ms after V_{CC} reaches its proper operating level. This recommendation is to ensure long-term reliability of the device.
CPUTYP	I	**CPU type** distinguishes the Primary processor from the Dual processor. In a single processor environment, or when the processor is acting as the Primary processor in a dual processing system, CPUTYP should be strapped to V_{SS}. The Dual processor should have CPUTYP strapped to V_{CC}.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock in which the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D/P#	O	The **dual/primary** processor indication. The Primary processor drives this pin low when it is driving the bus, otherwise it drives this pin high. D/P# is always driven. D/P# can be sampled for the current cycle with ADS# (like a status pin). This pin is defined only on the Primary processor. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies. Within these restrictions, two processors of different steppings may operate together in a system.
D63–D0	I/O	These are the 64 **data lines** for the processor. Lines D7–D0 define the least significant byte of the data bus; lines D63–D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.

† The pins are classified as Input or Output based on their function in Master Mode. See the *Pentium® Processor Family Developer's Manual* (order number 273204) for more information.

Table 4. Pin Quick Reference (Sheet 3 of 5)

Symbol	Type†	Name and Function
DP7–DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the Pentium processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the processor on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium processor. DP7 applies to D63–D56, DP0 applies to D7–D0.
[DPEN#] PICD0	I/O	**Dual processing enable** is an output of the Dual processor and an input of the Primary processor. The Dual processor drives DPEN# low to the Primary processor at RESET to indicate that the Primary processor should enable dual processor mode. DPEN# may be sampled by the system at the falling edge of RESET to determine if the dual-processor socket is occupied. DPEN# shares a pin with PICD0.
EADS#	I	The **external address strobe** signal indicates that a valid external address has been driven onto the processor address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the processor generates a write, and EWBE# is sampled inactive, the processor holds off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS-type floating-point error reporting. FERR# is never driven active by the Dual processor.
FLUSH#	I	When asserted, the **cache flush** input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle is generated by the processor to indicate completion of the write back and invalidation. When FLUSH# is sampled low when RESET transitions from high to low, three-state test mode is entered. If two Pentium processors are operating in dual processing mode and FLUSH# is asserted, the Dual processor performs a flush first (without a flush acknowledge cycle), then the Primary processor performs a flush followed by a flush acknowledge cycle. When the FLUSH# signal is asserted in dual processing mode, it must be deasserted at least one clock prior to BRDY# of the FLUSH Acknowledge cycle to avoid DP arbitration problems.
FRCMC#	I	The **functional redundancy checking master/checker** mode input is used to determine whether the processor is configured in master mode or checker mode. When configured as a master, the processor drives its output pins as required by the bus protocol. When configured as a checker, the processor three-states all outputs (except IERR# and TDO) and samples the output pins. The configuration as a master/checker is set after RESET and may not be changed other than by a subsequent RESET.
HIT#	O	The **inquire cycle hit/miss** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the processor data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the processor cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **inquire cycle hit/miss to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after an inquire cycle that results in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.

† The pins are classified as Input or Output based on their function in Master Mode. See the *Pentium® Processor Family Developer's Manual* (order number 273204) for more information.

Table 4. Pin Quick Reference (Sheet 4 of 5)

Symbol	Type†	Name and Function
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA is driven inactive and the processor resumes driving the bus. When the processor has a bus cycle pending, it is driven in the same clock in which HLDA is deasserted.
HOLD	I	In response to the **bus hold request**, the processor floats most of its output and input/output pins and asserts HLDA after completing all outstanding bus cycles. The processor maintains its bus in this state until HOLD is deasserted. HOLD is not recognized during LOCK cycles. The processor recognizes HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate two types of errors, internal parity errors and functional redundancy errors. When a parity error occurs on a read from an internal array, the processor asserts the IERR# pin for one clock and then shuts down. When the processor is configured as a checker and a mismatch occurs between the value sampled on the pins and the corresponding value computed internally, the processor asserts IERR# two clocks after the mismatched value is returned.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The processor does not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be deasserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock in which the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor issues ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI/LINT1	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated. When the local APIC is enabled, this pin becomes LINT1.
PBGNT#	I/O	When two Pentium processors are configured in dual processing mode, **Private bus grant** is the grant line that is used to perform private bus arbitration. PBGNT# should be left unconnected if only one Pentium processor exists in a system.
PBREQ#	I/O	When two Pentium processors are configured in dual processing mode, **Private bus request** is the request line that is used to perform private bus arbitration. PBREQ# should be left unconnected if only one Pentium processor exists in a system.
PCD	O	The **page cacheability disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page-by-page basis.
PCHK#	O	The **data parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned. When two Pentium processors are operating in dual processing mode, PCHK# may be driven two or three clocks after BRDY# is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception is taken as a result of a data parity error on a read cycle. When this pin is sampled active in the clock during which a data parity error is detected, the processor latches the address and control signals of the cycle with the parity error in the machine check registers. When PEN# is active and the machine check enable bit in CR4 is set to “1”, the processor vectors to the machine check exception before the beginning of the next instruction.

† The pins are classified as Input or Output based on their function in Master Mode. See the *Pentium® Processor Family Developer’s Manual* (order number 273204) for more information.

Table 4. Pin Quick Reference (Sheet 5 of 5)

Symbol	Type†	Name and Function
PHIT#	I/O	**Private inquire cycle hit/miss** is a hit indication used to maintain local cache coherency when two Pentium processors are configured in dual processing mode. PHIT# should be left unconnected if only one Pentium processor exists in a system.
PHITM#	I/O	**Private inquire cycle hit/miss to a modified line** is a hit indication used to maintain local cache coherency when two Pentium processors are configured in dual processing mode. PHITM# should be left unconnected if only one Pentium processor exists in a system.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the **processor interrupt controller clock** input of the processor.
PICD1/[DPEN#]–PICD0/[APICEN]	I/O	**Processor interrupt controller data lines 0–1** of the processor comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistors. These signals share pins with DPEN# and APICEN respectively.
PM1/BP1–PM0/BP0	O	These pins function as part of the performance monitoring feature. The breakpoint 1–0 pins are multiplexed with the **performance monitoring 1–0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine whether the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active, or Probe Mode being entered.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the processor, which causes the core to consume less power. When the processor recognizes STPCLK#, the processor stops execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generates a stop grant acknowledge cycle. When STPCLK# is asserted, the processor still responds to interprocessor and external snoop requests.
TCK	I	The **testability clock input** provides the clocking function for the Pentium processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
V_{CC}	I	The Pentium processor has 53 3.3 V **power** inputs.
V_{SS}	I	The Pentium processor has 53 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock in which the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **write back/write through** input allows a data cache line to be defined as write back or write through on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

† The pins are classified as Input or Output based on their function in Master Mode. See the *Pentium® Processor Family Developer's Manual* (order number 273204) for more information.

Table 5. Bus Frequency Selections

Pentium® Processor Core Frequency (max)	External Bus Frequency (max)	Bus/Core Ratio	BF1	BF0
166 MHz	66 MHz	2/5	0	0
133 MHz	66 MHz	1/2	1	0
100 MHz	66 MHz	2/3	1	1

2.1.4 Pin Reference Tables

Table 6. Output Pins

Name	Active Level[1]	When Floated
ADS#[2]	Low	Bus Hold, BOFF#
ADSC#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#–BE5#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#[2]	Low	Bus Hold, BOFF#
D/P#[3]	n/a	
FERR#[3]	Low	
HIT#[2]	Low	
HITM#[2]	Low	
HLDA[2]	High	
IERR#	Low	
LOCK#[2]	Low	Bus Hold, BOFF#
M/IO#[2], D/C#[2], W/R#[2]	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3–BP2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC[2]	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTES:
1. All output and input/output pins are floated during three-state test mode and checker mode (except IERR#).
2. These are I/O signals when two Pentium processors are operating in dual processing mode.
3. These signals are undefined when the processor is configured as a dual processor.

Table 7. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M#†	Low	Asynchronous		
AHOLD	High	Synchronous		
BF1–BF0	High	Synchronous/RESET	Pullup	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous		Bus State T2, T12, T2P
BRDYC#	Low	Synchronous	Pullup	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
CPUTYP	High	Synchronous/RESET		
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
FRCMC#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE#†	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
PICCLK	High	Asynchronous	Pullup	
R/S#	n/a	Asynchronous	Pullup	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

† Undefined when the processor is configured as a dual processor.

Table 8. Input/Output Pins

Name	Active Level	When Floated[1]	Qualified (when an input)	Internal Resistor
A31–A3	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
BE4#–BE0#	Low	Address Hold, Bus Hold, BOFF#	RESET	Pulldown[2]
D63–D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7–DP0	n/a	Bus Hold, BOFF#	BRDY#	
PICD0[DPEN#]				Pullup
PICD1[APICEN]				Pulldown

NOTES:
1. All output and input/output pins are floated during three-state test mode (except TDO) and checker mode (except IERR# and TDO).
2. BE3#–BE0# have pulldowns during RESET only.

Table 9. Inter-processor Input/Output Pins

Name†	Active Level	Internal Resistor
PHIT#	Low	Pullup
PHITM#	Low	Pullup
PBGNT#	Low	Pullup
PBREQ#	Low	Pullup

† For proper interprocessor operation, the system cannot load these signals.

2.1.5 Pin Grouping According to Function

Table 10. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF1–BF0
Address Bus	A31–A3, BE7#–BE0#
Address Mask	A20M#
Data Bus	D63–D0
Address Parity	AP, APCHK#
APIC Support	PICCLK, PICD1–PICD0
Data Parity	DP7–DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, ADSC#, BRDY#, BRDYC#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Dual Processing Private Bus Control	PBGNT#, PBREQ#, PHIT#, PHITM#
Interrupts	INTR, NMI
Floating-point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
Functional Redundancy Checking	FRCMC# (IERR#)
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3–BP2
Power Management	STPCLK#
Miscellaneous Dual Processing	CPUTYP, D/P#
Probe Mode	R/S#, PRDY

2.2 Mechanical Specifications

The embedded Pentium processor is packaged in a 296-pin ceramic staggered pin grid array (SPGA) package. The pins are arranged in a 37 x 37 matrix and the package dimensions are 1.95" x 1.95" (Table 11). Figure 4 and Table 12 show the package dimensions.

Table 11. Package Information Summary for Pentium® Processor

Package Type		Total Pins	Pin Array	Package Size
Ceramic Staggered Pin Grid Array	SPGA	296	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm

Figure 4. SPGA Package Dimensions

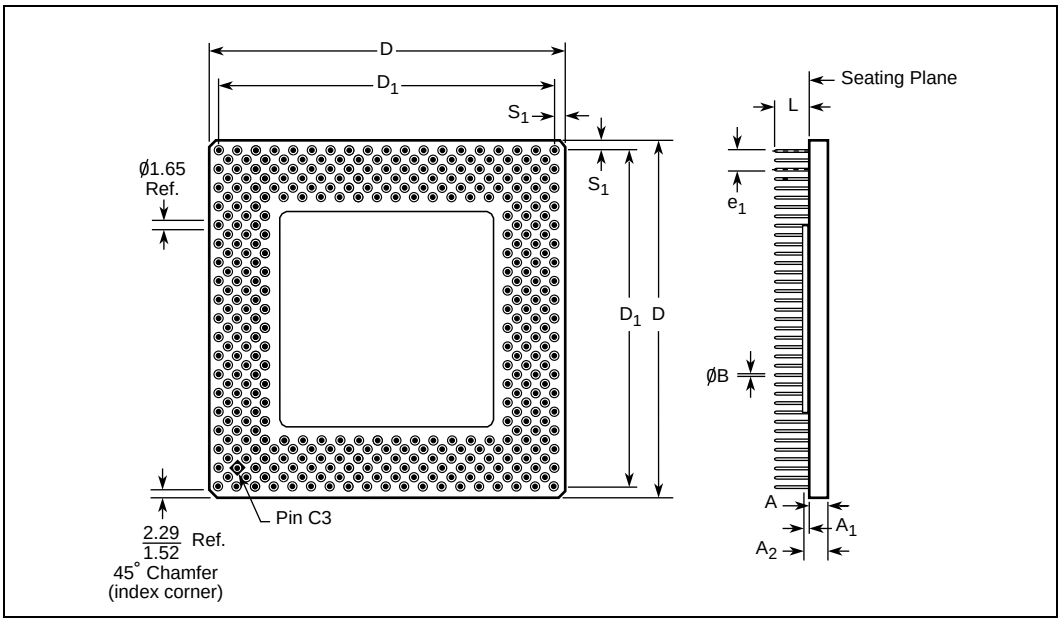


Table 12. SPGA Package Dimensions Key

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.62	2.97		0.103	0.117	
A_1	0.69	0.84	Metal Lid	0.027	0.033	Metal Lid
A_2	3.31	3.81	Metal Lid	0.130	0.150	Metal Lid
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D_1	45.59	45.85		1.795	1.805	
e_1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	296		Lead Count	296		Lead Count
S_1	1.52	2.54		0.060	0.100	

2.3 Thermal Specifications

The Pentium processor is specified for proper operation when case temperature, T_{CASE} (T_C), is within the specified range of 0° C to 70° C.

The power dissipation specification in Table 13 is provided for designing thermal solutions for operation at a sustained maximum level. This is the worst-case power the device would dissipate in a system. This number is used for design of a thermal solution for the device.

Table 13. Power Dissipation Requirements for Thermal Solution Design

Parameter	Typical[1]	Max	Unit	Notes
Active Power Dissipation	5.4 4.3 3.9	14.5[2] 11.2[3] 10.1[3]	Watts	166 MHz 133 MHz 100 MHz
Stop Grant and Auto Halt Powerdown Power Dissipation		2.1 1.7 1.55	Watts	166 MHz, Note 4 133 MHz, Note 4 100 MHz, Note 4
Stop Clock Power Dissipation	0.02	<0.3	Watts	Note 5

NOTES:
1. This is the typical power dissipation in a system. This value was the average value measured in a system using a typical device at nominal V_{CC} (3.3 V for 100 and 133 MHz processors and 3.5 V for 166 MHz processors) running typical applications. This value is highly dependent upon the specific system configuration.
2. Systems must be designed to thermally dissipate the maximum active power of the device. It is determined using a worst-case instruction mix with V_{CC}=3.5 V, and also takes into account the thermal time constants of the package.
3. Systems must be designed to thermally dissipate the maximum active power of the device. It is determined using a worst case instruction mix with V_{CC} = 3.3 V and also takes into account the thermal time constants of the package.
4. Stop Grant/Auto Halt Powerdown power dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
5. Stop Clock power dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.

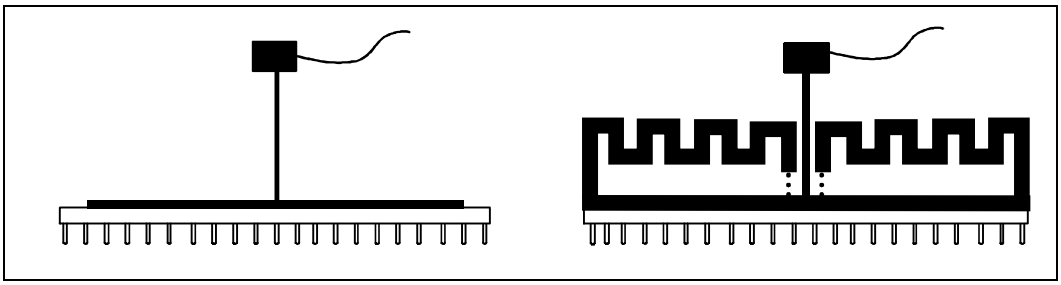
2.3.1 Measuring Thermal Values

To verify that the proper T_C (case temperature) is maintained, it should be measured at the center of the package top surface (opposite of the pins). The measurement is made in the same way with or without a heatsink attached. When a heatsink is attached, a hole (0.150" diameter or smaller) should be drilled through the heatsink to allow a probe to touch the center of the package. See Figure 5 for an illustration of how to measure T_C.

To minimize the measurement errors, use the following approach:

- Use 36-gauge or finer diameter K, T, or J type thermocouples.
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements.
- Attach the thermocouple at a 90-degree angle as shown in Figure 5.
- The hole size should be 0.150" or less in diameter.

Figure 5. Technique for Measuring Case Temperature (T_C)



2.3.2 Thermal Equations And Data

For the Pentium processor, an ambient temperature, T_A (air temperature around the processor), is not specified directly. The only restriction is that the case temperature (T_C) is met. To calculate T_A values, use the following equations:

$T_A = T_C - (P * \theta_{CA})$

$\theta_{CA} = \theta_{JA} - \theta_{JC}$

where:

T_A and T_C =	ambient and case temperature (°C)
θ_{CA} =	case-to-ambient thermal resistance (°C/W)
θ_{JA} =	junction-to-ambient thermal resistance (°C/W)
θ_{JC} =	junction-to-case thermal resistance (°C/W)
P =	maximum power consumption in Watts (see Table 13)

Table 14 lists the θ_{CA} values for the Pentium processor with passive heatsinks.

Thermal data collection parameters:

- Heatsinks are omnidirectional pin aluminum alloy
- Features were based on standard extrusion practices for a given height
- Pin size ranged from 50 to 129 mils
- Pin spacing ranged from 93 to 175 mils
- Base thickness ranged from 79 to 200 mils
- Heatsink attach was 0.005" of thermal grease
- Using an attach thickness of 0.002” improves performance by approximately 0.3 °C/W

Table 14. Thermal Resistances for Embedded Pentium® Processors

Heatsink Height in Inches	θ_{JC} (°C/Watt)	θ_{CA}(°C/Watt) vs. Laminar Airflow (Linear ft/min)					
		0	100	200	400	600	800
0.25	1.25	9.4	8.3	6.9	4.7	3.9	3.3
0.35	1.25	9.1	7.8	6.3	4.3	3.6	3.1
0.45	1.25	8.7	7.3	5.6	3.9	3.2	2.8
0.55	1.25	8.4	6.8	5.0	3.5	2.9	2.6
0.65	1.25	8.0	6.3	4.6	3.3	2.7	2.4
0.80	1.25	7.3	5.6	4.2	2.9	2.5	2.3
1.00	1.25	6.6	4.9	3.9	2.9	2.4	2.1
1.20	1.25	6.2	4.6	3.6	2.7	2.3	2.1
1.40	1.25	5.7	4.2	3.3	2.5	2.2	2.0
Without Heatsink	1.7	14.5	13.8	12.6	10.5	8.6	7.5

3.0 Electrical Specifications

This section describes the DC and AC specifications for the embedded Pentium processor.

3.1 3.3 V Power Supply

The processor has all V_{CC} 3.3-V inputs. The CLK and PICCLK inputs can tolerate a 5-V input signal. This allows the processor to use 5-V or 3.3-V clock drivers.

3.2 3.3 V Inputs and Outputs

The inputs and outputs of the processor are 3.3 V JEDEC standard levels. Both inputs and outputs are also TTL-compatible, although the inputs cannot tolerate voltage swings above the 3.3 V V_{IN} max. The CLK and PICCLK inputs of the processor are 5 V tolerant. This allows a 5-V clock driver to drive the processor. All other pins are 3.3 V only.

For processor outputs, if the system support components use TTL-compatible inputs, the components will interface to the processor without extra logic. This is because the processor drives according to the 5-V TTL specification (but not beyond 3.3 V).

For processor inputs, the voltage must not exceed the 3.3 V V_{IH3} maximum specification. System support components can consist of 3.3 V devices or open-collector devices. In an open-collector configuration, the external resistor can be biased with the processor's V_{CC}. As the processor's V_{CC} changes from 5 V to 3.3 V, so does this signal's maximum drive.

3.3 Absolute Maximum Ratings

Functional operating conditions are given in the AC and DC specification tables. Functional operation at the maximums is not implied or guaranteed. Extended operation beyond the maximum ratings may affect device reliability. Furthermore, although the Pentium processor contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only.

Table 15. Absolute Maximum Ratings

Parameter	Maximum Rating
Case temperature under bias	–65° C to 110° C
Storage temperature	–65° C to 150° C
3 V Supply voltage with respect to V_{SS}	–0.5 V to +4.6 V
3 V Only Buffer DC Input Voltage	–0.5 V to V_{CC} + 0.5; not to exceed V_{CC3} max[1]
5 V Safe Buffer DC Input Voltage	–0.5 V to 6.5 V[2,3]

NOTES:
1. Applies to all Pentium® processor inputs except CLK and PICCLK.
2. Applies to CLK and PICCLK.
3. See overshoot/undershoot transient specification.

3.4 DC Specifications

Tables 16–18 list the DC specifications that apply to the Pentium processor. The Pentium processor is a 3.3 V part internally. The CLK and PICCLK inputs may be 3.3 V or 5 V inputs. Since the 3.3 V (5 V-safe) input levels defined in Table 16 are the same as the 5 V TTL levels, the CLK and PICCLK inputs are compatible with existing 5 V clock drivers.

Table 16. 3.3 V DC Specifications

T_{CASE} = 0 to 70° C; 3.135 V < V_{CC} < 3.6 V for 100 and 133 MHz devices
T_{CASE} = 0 to 70° C; 3.4 V < V_{CC} < 3.6 V for 166 MHz (VRE device)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.3	0.8	V	TTL Level, Note 1
V_{IH3}	Input High Voltage	2.0	V_{CC}+0.3	V	TTL Level, Note 1
V_{OL3}	Output Low Voltage		0.4	V	TTL Level, Note 2, Note 1
V_{OH3}	Output High Voltage	2.4		V	TTL Level, Note 3, Note 1
I_{CC3}	Power Supply Current		4250 3400 3250	mA mA mA	166 MHz, Note 4 133 MHz, Note 4 100 MHz, Note 4

NOTES:
1. 3.3 V TTL levels apply to all signals except CLK and PICCLK.
2. Parameter measured at 4 mA.
3. Parameter measured at 3 mA.
4. This value should be used for power supply design. It was determined using a worst-case instruction mix and V_{CC} = 3.6 V. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes. For more information, refer to “Decoupling Recommendations” on page 32.

Table 17. 3.3 V (5 V-Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL5}	Input Low Voltage	–0.3	0.8	V	TTL Level†
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level†

† Applies to CLK and PICCLK only.

Table 18. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	Guaranteed by design.
C_O	Output Capacitance		20	pF	Guaranteed by design.
$C_{I/O}$	I/O Capacitance		25	pF	Guaranteed by design.
C_{CLK}	CLK Input Capacitance		15	pF	Guaranteed by design.
C_{TIN}	Test Input Capacitance		15	pF	Guaranteed by design.
C_{TOUT}	Test Output Capacitance		20	pF	Guaranteed by design.
C_{TCK}	Test Clock Capacitance		15	pF	Guaranteed by design.
I_{LI}	Input Leakage Current				$0 < V_{IN} < V_{CC3}$, This parameter is for input without pullup or pulldown.
I_{LO}	Output Leakage Current				$0 < V_{IN} < V_{CC3}$, This parameter is for input without pullup or pulldown.
I_{IH}	Input Leakage Current		200		V_{IN} = 2.4 V, This parameter is for input with pulldown.
I_{IL}	Input Leakage Current		–400		V_{IN} = 0.4 V, This parameter is for input with pullup.

3.5 AC Specifications

The AC specifications of the Pentium processor consist of setup times, hold times, and valid delays at 0 pF.

3.5.1 Private Bus

When two Pentium processor are operating in dual processor mode, a “private bus” exists to arbitrate for the processor bus and maintain local cache coherency. The private bus consists of two pinout changes:

1. Five pins are added: PBREQ#, PBGNT#, PHIT#, PHITM#, D/P#.
2. Ten output pins become I/O pins: ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, HIT#, HITM#, HLDA, SCYC.

The new pins are given AC specifications of valid delays at 0 pF, setup times, and hold times. Simulate with these parameters and their respective I/O buffer models to guarantee that proper timings are met.

The AC specification gives input setup and hold times for the ten signals that become I/O pins. These setup and hold times must only be met when a dual processor is present in the system.

3.5.2 Power and Ground

For clean on-chip power distribution, the Pentium processor has 53 V_{CC} (power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external V_{CC} and V_{SS} pins of the processor. On the circuit board all V_{CC} pins must be connected to a V_{CC} plane. All V_{SS} pins must be connected to a V_{SS} plane.

3.5.3 Decoupling Recommendations

Liberal decoupling capacitance should be placed near the processor. Transient power surges can occur when the processor is driving its address and data buses at high frequencies. This is most common when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by minimizing the length of the circuit board traces between the processor and the decoupling capacitors.

These capacitors should be evenly distributed around each component on the 3.3 V plane. Capacitor values should be chosen to ensure that they eliminate both low and high frequency noise components.

For the Pentium processor, the power consumption can transition from a low power level to a much higher level (or high-to-low power) very rapidly. A typical example is when entering or exiting the Stop Grant state. Other examples are when executing a HALT instruction (causing the processor to enter the Auto HALT Powerdown state) or when transitioning from HALT to the Normal state. All these examples may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µF range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point at which the regulated power supply output reacts to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor (on the 3.3 V plane) to ensure that the supply voltage stays within specified limits during changes in the supply current during operation.

3.5.4 Connection Specifications

All NC and INC pins must remain unconnected. For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active high inputs should be connected to ground.

3.5.5 AC Timing Tables

The AC specifications given in Table 19 and Table 20 consist of output delays, input setup requirements and input hold requirements for a 66-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 V for both “0” and “1” logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct processor operation. Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer models to account for signal flight time delays.

The following applies to all standard TTL signals used with the Pentium processor family:

- TTL input test waveforms are assumed to be 0 to 3 V transitions with 1 V/ns rise and fall times.
- 0.3 V/ns ≤ input rise/fall time ≤ 5 V/ns.

Table 19. AC Specifications (Sheet 1 of 3)

T_{CASE} = 0 to 70° C; 3.135 V < V_{CC} < 3.6 V for 100 and 133 MHz devices, C_L = 0 pF
T_{CASE} = 0 to 70° C; 3.4 V < V_{CC} < 3.6 V for 166 MHz (VRE device), C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz		
t_{1a}	CLK Period	15.0	30.0	ns	6	
t_{1b}	CLK Period Stability			ps		Adjacent Clocks, Notes 1, 21
t_2	CLK High Time	4.0		ns	6	2 V, Note 1
t_3	CLK Low Time	4.0		ns	6	0.8 V, Note 1
t_4	CLK Fall Time	0.15	1.5	ns	7	2.0 V–0.8 V, Note 1
t_5	CLK Rise Time	0.15	1.5	ns	6	0.8 V–2.0 V, Note 1
t_{6a}	PWT, PCD, CACHE# Valid Delay	1.0	7.0	ns	7	
t_{6b}	AP Valid Delay	1.0	8.5	ns	7	
t_{6c}	BE7#–BE0#, LOCK# Valid Delay	0.9	7.0	ns	7	
t_{6d}	ADS# Valid Delay	0.8	6.0	ns	7	
t_{6e}	ADSC#, D/C#, W/R#, SCYC, Valid Delay	0.8	7.0	ns	7	
t_{6f}	M/IO# Valid Delay	0.8	5.9	ns	7	
t_{6g}	A16–A3 Valid Delay	0.5	6.3	ns	7	
t_{6h}	A31–A17 Valid Delay	0.6	6.3	ns	7	
t_7	ADS#, ADSC#, AP, A31–A3, PWT, PCD, BE7#–BE0#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	8	1
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	7	3
t_{8b}	PCHK# Valid Delay	1.0	7.0	ns	7	3
t_{9a}	BREQ Valid Delay	1.0	8.0	ns	7	3
t_{9b}	SMIACT# Valid Delay	1.0	7.3	ns	7	3
t_{9c}	HLDA Valid Delay	1.0	6.8	ns	7	
t_{10a}	HIT# Valid Delay	1.0	6.8	ns	7	
t_{10b}	HITM# Valid Delay	0.7	6.0	ns	7	
t_{11a}	PM1–PM0, BP3–BP0 Valid Delay	1.0	10.0	ns	7	
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	7	
t_{12}	D63–D0, DP7–DP0 Write Data Valid Delay	1.3	7.5	ns	7	
t_{13}	D63–D0, DP3–DP0 Write Data Float Delay		10.0	ns	8	1
t_{14}	A31–A5 Setup Time	6.0		ns	9	22
t_{15}	A31–A5 Hold Time	1.0		ns	9	
t_{16a}	INV, AP Setup Time	5.0		ns	9	
t_{16b}	EADS# Setup Time	5.0		ns	9	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	9	
t_{18a}	KEN# Setup Time	5.0		ns	9	
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	9	

NOTE: See Table 21 for notes.

Table 19. AC Specifications (Sheet 2 of 3)

T_{CASE} = 0 to 70° C; 3.135 V < V_{CC} < 3.6 V for 100 and 133 MHz devices, C_L = 0 pF
T_{CASE} = 0 to 70° C; 3.4 V < V_{CC} < 3.6 V for 166 MHz (VRE device), C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	9	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		ns	9	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		ns	9	
t_{22}	AHOLD, BOFF# Setup Time	5.5		ns	9	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	9	
t_{24a}	BUSCHK#, EWBE#, HOLD Setup Time	5.0		ns	9	
t_{24b}	PEN# Setup Time	4.8		ns	9	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	9	
t_{25b}	HOLD Hold Time	1.5		ns	9	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	9	9, 12
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	9	10
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	9	9, 12, 13
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	9	10
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		11, 13
t_{31}	R/S# Setup Time	5.0		ns	9	9, 12, 13
t_{32}	R/S# Hold Time	1.0		ns	9	10
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		11, 13
t_{34}	D63–D0, DP7–DP0 Read Data Setup Time	2.8		ns	9	
t_{35}	D63–D0, DP7–DP0 Read Data Hold Time	1.5		ns	9	
t_{36}	RESET Setup Time	5.0		ns	10	8, 9, 12
t_{37}	RESET Hold Time	1.0		ns	10	8, 10
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	10	8, 13
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		ms	10	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time	5.0		ns	10	9, 12, 13
t_{41}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Hold Time	1.0		ns	10	10
t_{42a}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time, Async.	2.0		CLKs	10	To RESET falling edge, Note 12
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#, BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLKs	10	To RESET falling edge, Note 23
t_{42d}	Reset Configuration Signal BRDYC# Hold Time, RESET driven synchronously	1.0		ns		To RESET falling edge, 1, 23
t_{43a}	BF, CPUTYP Setup Time	1.0		ms	10	To RESET falling edge, Note 18
t_{43b}	BF, CPUTYP Hold Time	2.0		CLKs	10	To RESET falling edge, Note 18

NOTE: See Table 21 for notes.

Table 19. AC Specifications (Sheet 3 of 3)

T_{CASE} = 0 to 70° C; 3.135 V < V_{CC} < 3.6 V for 100 and 133 MHz devices, C_L = 0 pF
T_{CASE} = 0 to 70° C; 3.4 V < V_{CC} < 3.6 V for 166 MHz (VRE device), C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{43c}	APICEN, BE4# Setup Time	2.0		CLKs	10	To RESET falling edge
t_{43d}	APICEN, BE4# Hold Time	2.0		CLKs	10	To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		ns	6	
t_{46}	TCK High Time	25.0		ns	6	2 V, Note 1
t_{47}	TCK Low Time	25.0		ns	6	0.8 V, Note 1
t_{48}	TCK Fall Time		5.0	ns	6	2.0 V–0.8 V, Notes 1,5,6
t_{49}	TCK Rise Time		5.0	ns	6	0.8 V–2.0 V, Notes 1,5,6
t_{50}	TRST# Pulse Width	40.0		ns	12	Asynchronous, Note 1
t_{51}	TDI, TMS Setup Time	5.0		ns	11	4
t_{52}	TDI, TMS Hold Time	13.0		ns	11	4
t_{53}	TDO Valid Delay	3.0	20.0	ns	11	5
t_{54}	TDO Float Delay		25.0	ns	11	1, 5
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	ns	11	2, 5, 7
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	11	1, 2, 5, 7
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	11	2, 4, 7
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	11	2, 4, 7
APIC AC Specifications						
t_{60a}	PICCLK Frequency	2.0	16.66	MHz		
t_{60b}	PICCLK Period	60.0	500.0	ns	6	
t_{60c}	PICCLK High Time	15.0		ns	6	
t_{60d}	PICCLK Low Time	15.0		ns	6	
t_{60e}	PICCLK Rise Time	0.15	2.5	ns	6	
t_{60f}	PICCLK Fall Time	0.15	2.5	ns	6	
t_{60g}	PICD1–PICD0 Setup Time	3.0		ns	9	To PICCLK
t_{60h}	PICD1–PICD0 Hold Time	2.5		ns	9	To PICCLK
t_{60i}	PICD1–PICD0 Valid Delay (LtoH)	4.0	38.0	ns	7	From PICCLK, Notes 24, 25
t_{60j}	PICD1–PICD0 Valid Delay (HtoL)	4.0	22.0	ns	7	From PICCLK, Notes 24, 25
t_{61}	PICCLK Setup Time	5.0		ns		To CLK, Note 26
t_{62}	PICCLK Hold Time	2.0		ns		To CLK, Note 26
t_{63}	PICCLK Ratio (CLK/PICCLK)	4				27

NOTE: See Table 21 for notes.

Table 20. Dual Processor Mode AC Specifications

T_{CASE} = 0 to 70° C; 3.135 V < V_{CC} < 3.6 V for 100 and 133 MHz devices, C_L = 0 pF
T_{CASE} = 0 to 70° C; 3.4 V < V_{CC} < 3.6 V for 166 MHz (VRE device), C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{80a}	PBREQ#, PBGNT#, PHIT# Flight Time	0	2.0	ns		20, 25
t_{80b}	PHITM# Flight Time	0	1.8	ns		20, 25
t_{83a}	A31–A5 Setup Time	3.7		ns	9	14, 17, 22
t_{83b}	D/C#, W/R#, CACHE#, LOCK#, SCYC Setup Time					
t_{83c}	ADS#, M/IO# Setup Time	5.8		ns	9	14, 17
t_{83d}	HIT#, HITM# Setup Time	6.0		ns	9	14, 17
t_{83e}	HLDA Setup Time	6.0		ns	9	14, 17
t_{84}	ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, A31–A5, HLDA, HIT#, HITM#, SCYC Hold Time	1.0		ns	9	14, 17
t_{85}	DPEN# Valid Time		10.0	CLKs		14, 15, 19
t_{86}	DPEN# Hold Time	2.0		CLKs		14, 16, 19
t_{87}	APIC ID (BE3#–BE0#) Setup Time	2.0		CLKs	10	To RESET falling edge, Note 19
t_{88}	APIC ID (BE3#–BE0#) Hold Time	2.0		CLKs	10	From RESET falling edge, Note 19
t_{89}	D/P# Valid Delay	1.0	8.0	ns	7	Primary Processor Only

NOTE: See Table 21 for table notes.

Table 21. Notes for Tables 19 and 20

1. Not 100% tested. Guaranteed by design/characterization.
2. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
3. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions.
4. Referenced to TCK rising edge.
5. Referenced to TCK falling edge.
6. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
7. During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).
8. FRCMC# should be tied to V_{CC} (high) to ensure proper operation of the Pentium processor as a primary processor.
9. Setup time is required to guarantee recognition on a specific clock. The Pentium processor must meet this specification for dual processor operation for the FLUSH# and RESET signals.
10. Hold time is required to guarantee recognition on a specific clock. The Pentium processor must meet this specification for dual processor operation for the FLUSH# and RESET signals.
11. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
12. This input may be driven asynchronously. However, when operating two processors in dual processing mode, FLUSH# and RESET must be asserted synchronously to both processors.
13. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be deasserted (inactive) for a minimum of two clocks before being returned active.
14. Timings are valid only when dual processor is present.
15. Maximum time DPEN# is valid from rising edge of RESET.
16. Minimum time DPEN# is valid after falling edge of RESET.
17. The D/C#, M/IO#, W/R#, CACHE#, and A31–A5 signals are sampled only on the CLK during which ADS# is active.
18. BF and CPUTYP should be strapped to V_{CC} or V_{SS}.
19. RESET is synchronous in dual processing mode and functional redundancy checking mode. All signals that have a setup or hold time with respect to a falling or rising edge of RESET in UP mode should be measured with respect to the first processor clock edge in which RESET is sampled either active or inactive in dual processing and functional redundancy checking modes.
20. The PHIT# and PHITM# signals operate at the core frequency.
21. These signals are measured on the rising edge of adjacent CLKs at 1.5 V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
22. In dual processing mode, timing t_{14} is replaced by t_{83a}. Timing t_{14} is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active) in both uniprocessor and dual processor modes.
23. BRDYC# and BUSCHK# are used as reset configuration signals to select buffer size.
24. This assumes an external pullup resistor to V_{CC} and a lumped capacitive load. The pullup resistor must be between 300 Ohms and 1 KOhms, the capacitance must be between 20 pF and 120 pF, and the RC product must be between 3 ns and 36 ns. V_{OL} for PICD1–PICD0 is 0.55 V.
25. This is a flight time specification that includes both flight time and clock skew. The flight time is the time from when the unloaded driver crosses 1.5 V (50% of min. V_{CC}), to when the receiver crosses the 1.5 V level (50% of min. V_{CC}). See Figure 13.
26. This is for the lock-step operation of the component only. This guarantees that APIC interrupts will be recognized on specific clocks to support two processors running in a lock step fashion, including FRC mode. FRC on the APIC pins is not supported but mismatches on these pins will result in a mismatch on other pins of the CPU.
27. The CLK to PICCLK ratio for lock-step operation must be an integer and the ratio (CLK/PICCLK) cannot be smaller than 4:1.

Figure 6. Clock Waveform

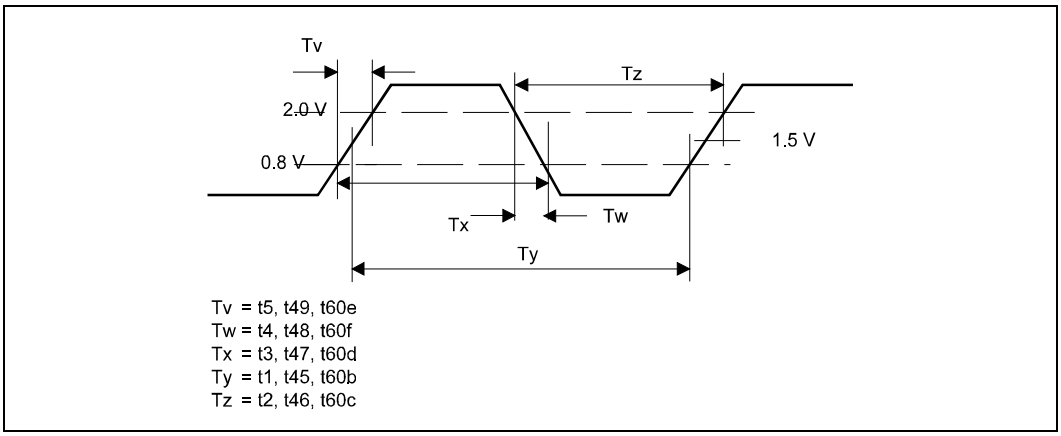


Figure 7. Valid Delay Timings

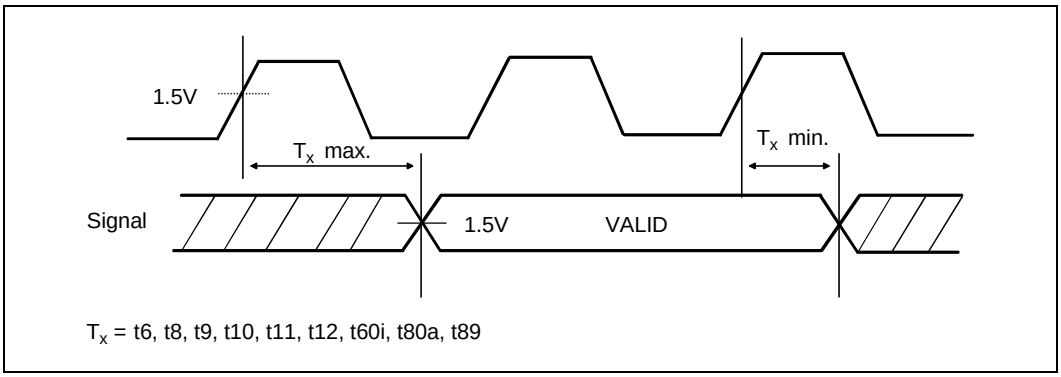


Figure 8. Float Delay Timings

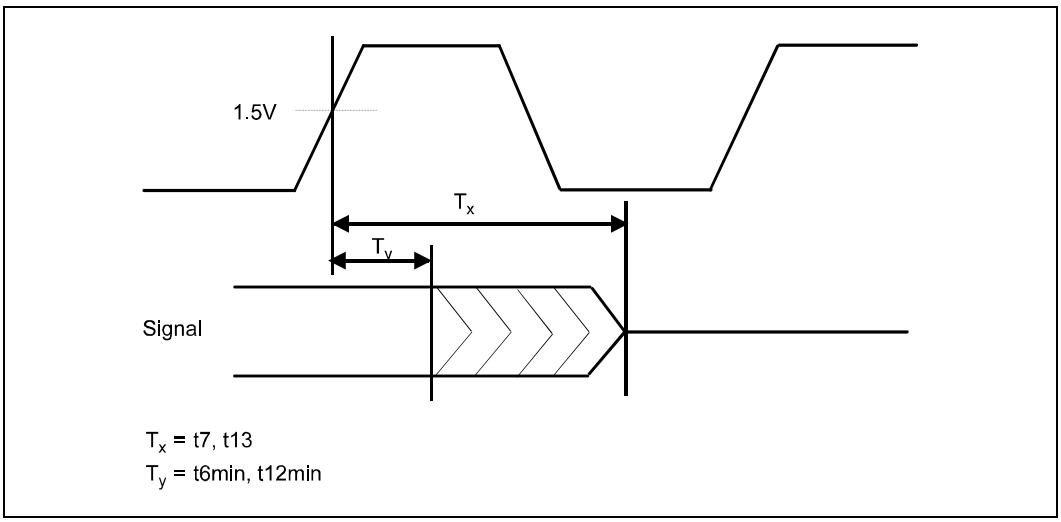
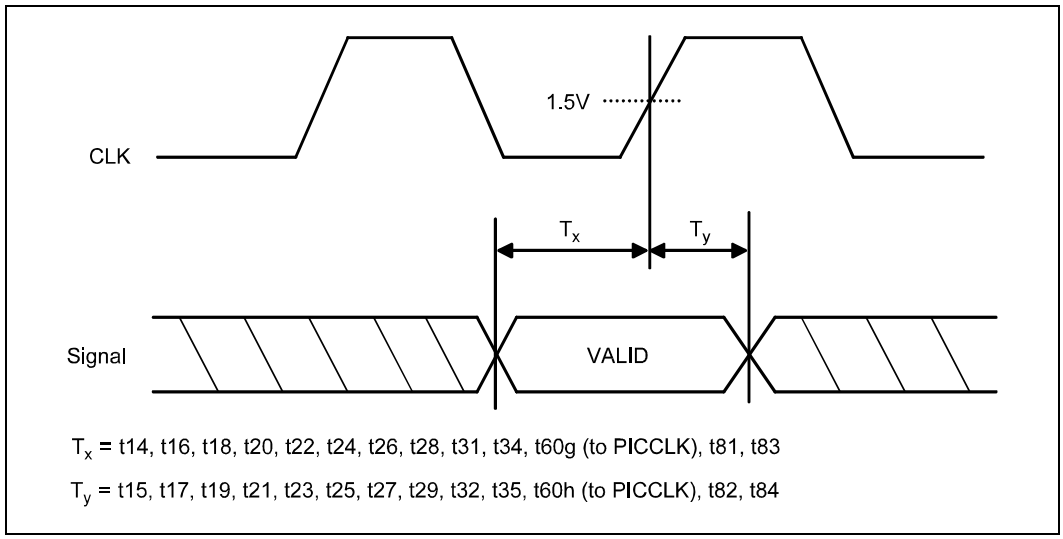


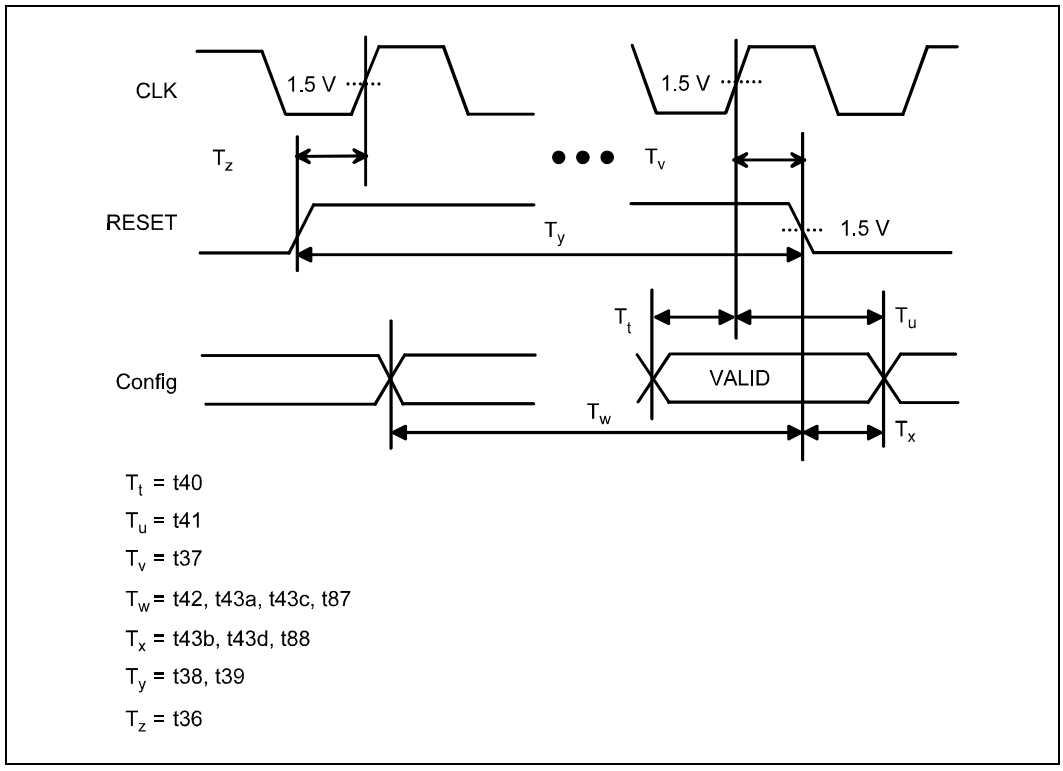
Figure 9. Setup and Hold Timings



T_x = t14, t16, t18, t20, t22, t24, t26, t28, t31, t34, t60g (to PICCLK), t81, t83

T_y = t15, t17, t19, t21, t23, t25, t27, t29, t32, t35, t60h (to PICCLK), t82, t84

Figure 10. Reset and Configuration Timings



T_t = t40

T_u = t41

T_v = t37

T_w = t42, t43a, t43c, t87

T_x = t43b, t43d, t88

T_y = t38, t39

T_z = t36

Figure 11. Test Timings

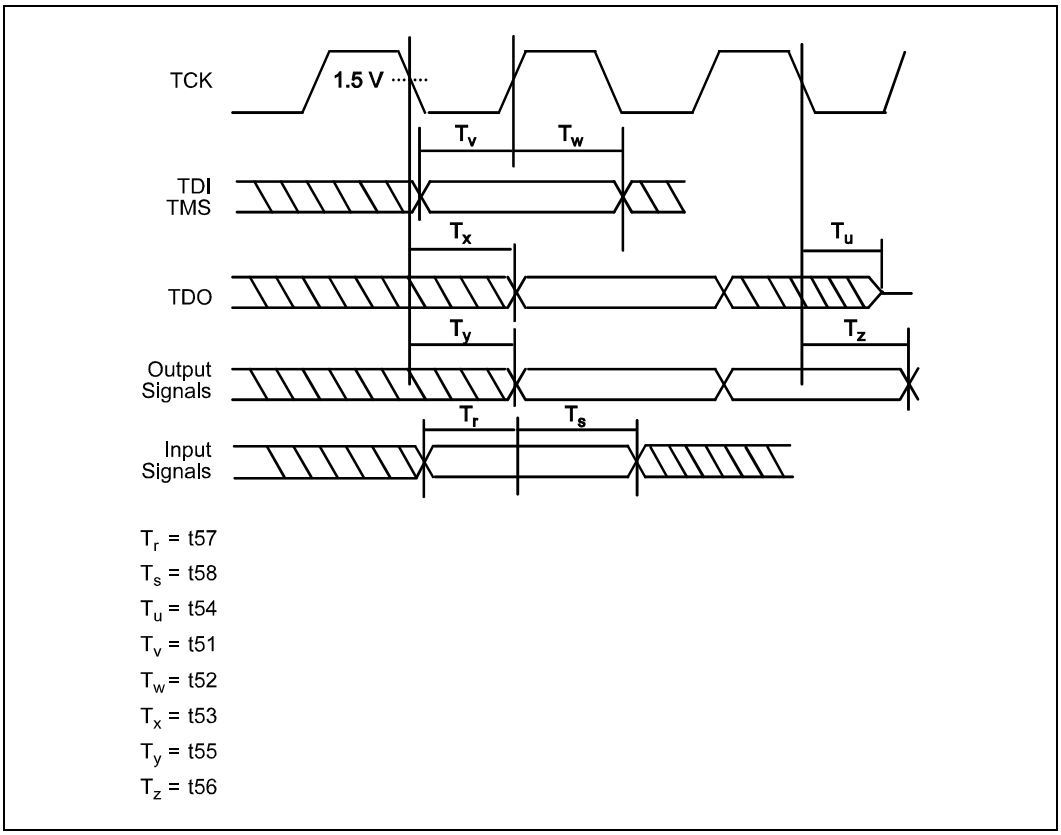


Figure 12. Test Reset Timings

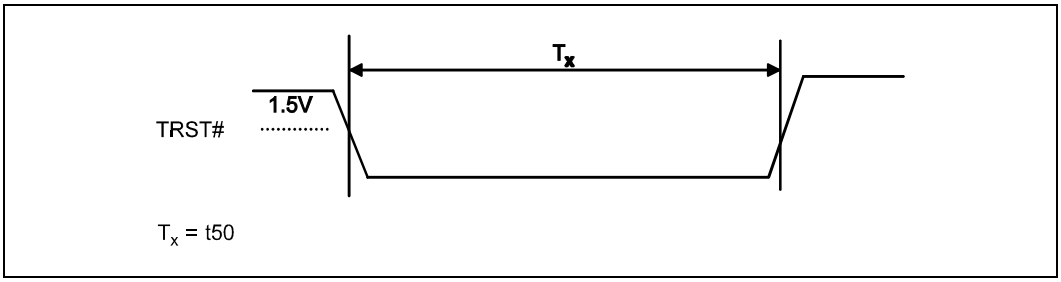


Figure 13. 50% V_{CC} Measurement of Flight Time